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| PATEL, DHARTI HARIDAS | |

| ART UNIT | PAPER NUMBER |
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| 2836 | |

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/501,651 | MA ET AL. | |
| | Examiner | Art Unit | |
| | Dharti H. Patel | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-3, 7, 12-14, 21, 25-26 and 28 are rejected under 35 U.S.C. 102(b) as being unpatentable over McClure et al., Patent No. 5,774,318. With respect to claim 1, McClure et al. teaches an electrostatic discharge protection circuit [Fig. 2] coupled to ground [Fig. 2, 104] comprising: an input [Fig. 2, Vcc 102]; a diode string [Fig. 2, 100] coupled to the input; a transistor switch [Fig. 2, Q3, 106] having its gate coupled to the diode string, the transistor switch coupling the input to ground in parallel to the diode string; and a reverse diode [Fig. 2, 116] coupling ground to the input as disclosed in Col. 3, lines 19-25 and lines 44-48.

With respect to claim 2, McClure teaches an electrostatic discharge protection circuit [alternatively shown in second embodiment, Fig. 3] where the switching transistor [Fig. 3, 106] comprises a Darlington pair [Fig. 3, Q4 and Q5] as disclosed in Col. 5, lines 55-62. In this embodiment, all the above-mentioned reference numerals to designate the previously mentioned components are the same as in the previous embodiment.

With respect to claim 3, McClure teaches an electrostatic discharge protection circuit [Fig. 2] where the switching transistor [Fig. 2, 106] comprises a bipolar transistor [Fig. 2, Q3].

With respect to claim 7, McClure teaches that the diode string [Fig. 2, 100] is forward biased on the application of positive ESD events at the input [Fig. 2, Vcc], [Col. 3, lines 19-25] and the reverse diode [Fig. 2, 116] is forward biased on the application of negative ESD events at the input [Col. 5, lines 7-16, Col. 6, lines 18-21].

With respect to claim 12, McClure teaches a method for providing electrostatic discharge protection comprising sinking a first type of ESD event to ground [Fig. 1, GND 104] from an input [Fig. 1, Vcc, 102] through a diode string [Fig. 1, 100] coupled to the input by triggering a transistor switch [Fig. 1, Q3, 106] having its gate coupled to the diode string, the transistor switch coupling the input to ground in parallel to the diode string; and sinking a second type of ESD event through a reverse diode [Fig. 1, 116] coupling ground to the input [Col. 3, lines 19-25, lines 38-41, lines 44-48, Col. 5, lines 7-16, Col. 6, lines 18-21].

With respect to claim 13, McClure teaches that the first type of ESD event is a positive voltage surge applied to the input [Col. 3, lines 19-25, lines 38-41], and the second type of ESD event is a negative voltage surge applied to the input [Col. 5, lines 7-16, Col. 6, lines 18-21].

With respect to claim 14, McClure teaches that triggering the transistor switch comprises triggering a Darlington pair [Fig. 3, Q4, Q5, 106].

With respect to claim 21, McClure teaches that the diode string [Fig. 2, 100] is comprised of a plurality of BC junction diodes [Fig. 3, 115].

With respect to claim 25, McClure teaches an ESD protected bonding pad comprising a first pad [Fig. 2, Vcc, 102]; a diode string [Fig. 2, 100] coupled to the first pad; a transistor switch [Fig. 2, Q3, 103] having its gate coupled to the diode string, the transistor switch coupling the first pad to ground in parallel to the diode string; and a reverse diode [Fig. 2, 116] coupling ground to the first pad as disclosed in Col. 3, lines 19-25 and lines 44-48.

With respect to claim 26, McClure teaches an ESD protected integrated circuit input comprising an integrated circuit input [Fig. 2, Vcc, 102]; a diode string [Fig. 2, 100] coupled to the integrated circuit input; a transistor switch [Fig. 2, Q3, 106] having its gate coupled to the diode string, the transistor switch coupling the integrated circuit input to ground in parallel to the diode string; and a reverse diode [Fig. 2, 116] coupling ground to the integrated circuit input as disclosed in Col. 3, lines 19-25 and lines 44-48.

With respect to claim 28, McClure teaches that the diode string [Fig. 2, 100] comprises one or more diode [Fig. 2, diodes 105] in series.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4-5, 16-17, 22 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClure et al., Patent No. 5,774,318, in view of Weiss, Patent No. 6,600,356. McClure teaches an ESD protection circuit coupled to ground, but does not disclose that the ESD protection circuit further comprises a capacitive element in series with the switching transistor to reduce the capacitance contributed by the switching transistor.

Weiss teaches an ESD protection circuit that comprises a diode string [Fig. 5, 10] and a switching transistor [Fig. 5, Q1]. Weiss further teaches a capacitive element [Fig. 4, D1] in series with the switching transistor [Fig. 4, Q1] to reduce the capacitance contributed by the switching transistor as disclosed in Col. 3, lines 12-30.

Both teachings are related by being electrostatic discharge protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Weiss, which teaches a capacitive element in series with a switching transistor, with the ESD protection circuit of McClure for the benefit of reducing the susceptibility to power supply transients.

With respect to claim 5, Weiss teaches that the switching transistor comprises a single bipolar transistor [Fig. 4, Q1] and the capacitive element comprises a diode [Fig. 4, D1], but does not disclose that the switching transistor comprises a Darlington pair. McClure teaches that a Darlington pair [Fig. 3, Q4, Q5, 106] is preferred over a single transistor [Fig. 2, Q3, 106, Col. 5, lines 55-65].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the switching transistor [Fig. 4, Q1] taught by Weiss with the switching transistor [Fig. 3, Q4, Q5, 106] to have a Darlington pair and a diode in series, because the Darlington pair offers a higher gain and thus a faster turn-on time, as well as a higher collector impedance which results in a lower leakage current.

With respect to claim 16, Weiss teaches an ESD protection circuit that comprises coupling the input [Fig. 5, V+] to ground [Fig. 5, GND] during ESD protection by means of a capacitive element [Fig. 4, D1] in series with the transistor switch [Fig. 4, Fig. 5, Q1] to reduce the capacitance contributed from the transistor switch [Col. 3, lines 12-30].

With respect to claim 17, Weiss teaches an ESD protection circuit that comprises coupling the input [Fig. 5, V+] to ground [Fig. 5, GND] during ESD protection by means of a capacitive element [Fig. 4, D1] in series with the transistor switch [Fig. 4, Fig. 5, Q1] to reduce the capacitance contributed from the transistor switch [Col. 3, lines 12-30], but does not disclose a diode in series with a Darlington pair to reduce the capacitance contributed from the Darlington pair.

McClure teaches that a Darlington pair [Fig. 3, Q4, Q5, 106] is preferred over a single transistor [Fig. 2, Q3, 106, Col. 5, lines 55-65]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the switching transistor [Fig. 4, Q1] taught by Weiss with the

switching transistor [Fig. 3, Q4, Q5, 106] to have a Darlington pair and a diode in series to reduce the capacitance contributed from the transistor switch, because the Darlington pair offers a higher gain and thus a faster turn-on time, as well as a higher collector impedance which results in a lower leakage current.

With respect to claim 22, the limitation is the polar opposite of claim 21, and is an art recognized equivalent configuration.

With respect to claim 29, Weiss teaches an ESD protection circuit that further comprises a resistor [Fig. 5, $R_{BE}$] coupled between the gate of the transistor switch [Fig. 5, Q1] and the diode string [Fig. 5, 10] on one hand and ground [Fig. 5, GND] on the other hand. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Weiss, which teaches a resistor coupled between the gate of the transistor switch and the diode string, with the ESD protection circuit of McClure because resistor connected to ground keeps triggering the switching transistor off under normal working conditions and also influences the duration of switch-off time of the switching transistor during an ESD event.

3. Claims 6 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over McClure et al., Patent No. 5,774,318, in view of Ring, Patent No. 3,755,751. McClure teaches an ESD protection circuit coupled to ground but does not disclose that the ESD circuit further comprises a series diode and a series resistor combined in any order and coupled between the gate of the transistor switch and the diode string on one hand and ground on the other hand.

Ring teaches a protection circuit for limiting the temperature of an amplifier circuit. The protection circuit comprises a series diode [Fig. 1, 68] and a series resistor [Fig. 1, 70] in any order and coupled between the gate of the transistor switch [Fig. 1, 118].

Both teachings are related by being protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ring, which teaches a series diode and a series resistor, with the ESD protection circuit of McClure because the resistor connected to ground keeps triggering the switching transistor off under normal working conditions and also influences the duration of switch-off time of the switching transistor during an ESD event and the use of diode insures that a stray current will now flow from the ground into the base of the switching transistor. In this configuration, the series diode [Ring, Fig. 1, 68] and series resistor [Ring, Fig. 1, 70] and the diode string [McClure, Fig. 1, 100] would be on one hand and ground [McClure, Fig. 1, GND] on the other hand.

With respect to claim 15, McClure teaches that triggering the Darlington pair [Fig. 3, 106] comprises coupling the first type of ESD event through the diode string [Fig. 3, 100] to the gate of the Darlington pair. Ring teaches that triggering the transistor switch comprises coupling the first type of ESD event through the diode string [Fig. 1, 66] to a series diode [Fig. 1, 68] and resistor [Fig. 1, 70] to ground to prevent ESD protection circuit from turning on during low to

moderate RF power operation, therefore minimizing leaking current and improving linearity.

4. Claims 8 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClure et al., Patent No. 5,774,318, in view of Brennan et al., Publication No. US2002/0130392. McClure teaches an ESD protection circuit coupled to ground that comprises a diode string, transistor switch and reverse diode, but does not disclose that the diode string, transistor switch and reverse diode is fabricated in GaAs, InP, SiGe, or other compound semiconductor.

Brennan teaches an ESD protection circuit [Fig. 20] that uses SiGe transistors, and SiGe diodes [Page 3, paragraph 35]. Both teachings are related by being electrostatic discharge protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Brennan, which teaches transistors and diodes fabricated in SiGe, with the ESD protection circuit of McClure for the benefit of using fabricated ESD resistant SiGe devices in either high-frequency ESD protection circuits or for high-frequency driver/receiver (D/R) circuits.

With respect to claim 23, McClure teaches that the diode string is comprised of a plurality of isolated implanted base collector diodes [Fig. 3, 100, 115], but does not disclose that the base collector diodes are fabricated in compound semiconductor technology, including GaAs, InP or other compound semiconductor. Brennan teaches an ESD protection circuit [Fig. 20] that uses SiGe transistors, and SiGe diodes [Page 3, paragraph 35].

5. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClure et al., Patent No. 5,774,318, in view of Johnson, Patent No. 6,624,999. McClure teaches an ESD protection circuit coupled to ground but does not disclose that the ESD protection circuit is coupled to an RF integrated circuit.

Johnson teaches an ESD protection circuit [Fig. 1, 35-1, 35-2], which is coupled to an RF integrated circuit [Fig. 1, 20, Col. 1, lines 54-55, lines 62-64]. Both teachings are related by being electrostatic discharge protection circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Johnson, which teaches an ESD protection circuit coupled to an RF integrated circuit, with the ESD protection circuit of McClure for the benefit of protecting an integrated circuit operating at a high frequency.

With respect to claim 10, Johnson teaches that the RF integrated circuit [Fig. 1, 20] comprises a power amplifier [Col. 2, lines 2-5].

6. Claims 11 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClure et al., Patent No. 5,774,318, in view of Weiss, Patent No. 6,600,356 as applied to claims 1-5 above, and further in view of Ring, Patent No. 3,755,751. With respect to claim 11, McClure teaches an ESD protection circuit coupled to ground comprises an input [Fig. 3, Vcc, 102]; a diode string [Fig. 3, 100] coupled to the input; a Darlington pair [Fig. 3, 106] having its gate coupled to the diode string, the Darlington pair coupling the input to ground in

parallel to the diode string; and a reverse diode [Fig. 3, 116] coupling ground to the input where the diode string is forward biased on the application of positive ESD events at the input and the reverse diode is forward biased on the application of negative ESD events at the input [Col. 3, lines 19-25, 44-48, Col. 5, lines 7-16, Col. 6, lines 18-21]. However, McClure does not disclose a series diode, a series resistor and a diode in series with the Darlington pair to reduce the capacitance contributed by the Darlington pair.

With respect to the limitation of a diode in series with a Darlington pair, Weiss teaches an ESD protection circuit that comprises coupling the input [Fig. 5, V+] to ground [Fig. 5, GND] during ESD protection by means of a capacitive element [Fig. 4, D1] in series with the transistor switch [Fig. 4, Fig. 5, Q1] to reduce the capacitance contributed from the transistor switch [Col. 3, lines 12-30], but does not disclose a diode in series with a Darlington pair to reduce the capacitance contributed from the Darlington pair.

McClure teaches that a Darlington pair [Fig. 3, Q4, Q5, 106] is preferred over a single transistor [Fig. 2, Q3, 106, Col. 5, lines 55-65]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the switching transistor [Fig. 4, Q1] taught by Weiss with the switching transistor [Fig. 3, Q4, Q5, 106] to have a Darlington pair and a diode in series to reduce the capacitance contributed by the Darlington pair, because the Darlington pair offers a higher gain and thus a faster turn-on time, as well as a higher collector impedance which results in a lower leakage current.

Ring teaches a series diode [Fig. 1, 68] and a series resistor [Fig. 1, 70], where the series diode and the series resistor are coupled in series with each other and their combination is coupled between the gate of the Darlington pair (taught by McClure).

All three teachings are related by being protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ring, which teaches a series diode and a series resistor, with the ESD protection circuit of McClure modified by Weiss, because the resistor connected to ground keeps triggering the switching transistor off under normal working conditions and also influences the duration of switch-off time of the switching transistor during an ESD event and the use of diode ensures that a stray current will not flow from the ground into the base of the switching transistor. In this configuration, the series diode [Ring, Fig. 1, 68] and series resistor [Ring, Fig. 1, 70] and the diode string [McClure, Fig. 1, 100] would be on one hand and ground [McClure, Fig. 1, GND] on the other hand.

With respect to claim 18, McClure teaches a method for providing ESD protection comprising sinking a first type of ESD event to ground [Fig. 3, 104] from an input through a diode string [Fig. 3, 100] coupled to the input by triggering a Darlington pair [Fig. 3, 106], the Darlington pair coupling the input to ground in parallel to the diode string; and a second type of ESD event through a reverse diode [Fig. 3, 116] coupling ground to the input. However, McClure does not disclose a series diode, a series resistor, and a diode in series with the

Darlington pair to reduce the capacitance contributed to the diode string from the Darlington pair.

Weiss teaches coupling the input [Fig. 4, V+] to ground [Fig. 4, GND] during the ESD protection by means of a diode [Fig. 4, D1] in series with the Darlington pair (or a switching transistor) to reduce the capacitance contributed to the diode string from the Darlington pair.

Ring teaches coupling the first type of ESD event through the diode string [Fig. 1, 66] to a series diode [Fig. 1, 68] and resistor [Fig. 1, 70] to ground [Fig. 1, Vcc] to prevent the ESD protection circuit from turning on during low to moderate RF power operation, therefore minimizing leaking current and improving linearity.

With respect to claim 19, McClure teaches that the first type of ESD event is a positive voltage surge applied to the input [Fig. 2, Vcc, 102, Col. 3, lines 19-25], and the second type of ESD event is a negative voltage surge applied to the input [Col. 5, lines 7-16, Col. 6, lines 18-21].

With respect to claim 20, the limitation is the polar opposite of claim 19, and is an art recognized equivalent configuration.

7. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over McClure et al., Patent No. 5,774,318, in view of Voldman et al., Patent No. 6,549,061. McClure teaches an ESD protection circuit that comprises a bipolar transistor [Fig. 2, 106] coupled to the input, but does not disclose that ESD protection circuit further comprises at least one heterojunction bipolar transistor coupled to the input.

Voldman teaches an ESD power clamp circuit. Voldman teaches at least one heterojunction bipolar transistor [Fig. 3, 202] coupled to the input [Fig. 3, 210]. Both teachings are related by being electrostatic discharge protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Voldman, which teaches at least one heterojunction bipolar transistor, with the ESD protection circuit of McClure because functional heterojunction bipolar transistor have some intrinsic ESD protection capabilities, allows reduced sizes and lower power supply voltages.

8. Claims 27 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClure, Patent No. 5,774,318, in view of Voldman, Patent No. 5,945,713. McClure teaches an ESD protection circuit coupled to ground, but does not disclose that chip-layout size of the transistor switch and diode string when used in combination is smaller than the chip-layout size of a diode string when used alone.

Voldman teaches an electrostatic discharge protection circuit. Voldman teaches that the transistor switch and diode string each have a chip-layout size and where the chip-layout size of the transistor switch and diode string when used in combination is smaller than the chip-layout size of a diode string when used alone, which used-alone diode string provides substantially the same ESD protection as the transistor switch and diode string in combination as

characterized by the maximum clamping voltage of the ESD protection circuit [Col. 3, lines 44-50].

Both teachings are related by being ESD protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Voldman with the ESD protection circuit of McClure in order to avoid electrical overstress and prevent undesirable current leakage paths that create system-level power loss.

With respect to claim 30, it would have been obvious to one of ordinary skill in the art to place the ESD circuit where there is a space to accommodate the circuit and its required electrical connections.

9. ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
01/30/2006

PHUONG T. VU
PRIMARY EXAMINER